IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RAMBUS, INC.,

Plaintiff,

v.

LSI CORPORATION,

Defendant.

_____/

RAMBUS, INC.,

Plaintiff,

v.

STMICROELECTRONICS N.V., and STMICROELECTRONICS, INC.,

Defendants.

_____/

No. C 10-05446 RS
No. C 10-05449 RS

CLAIM CONSTRUCTION ORDER

I. INTRODUCTION

This claim construction is only the latest salvo in a long-standing patent war over Dynamic Random Access Memory ("DRAM"), initiated by patentee Rambus against the many suppliers of constituent technologies. Defendants LSI Corporation and STMicroelectronics furnish chip makers with "memory controllers," which generally facilitate communications between the processor and the DRAM, and which allegedly infringe ten Rambus patents from the heavily-litigated Farmwald-

Horowitz family of patents, including U.S. Patent No. 6,426,916 ("the '916 patent").[1] Pursuant to *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996), and Patent Local Rule 4-3, the parties have presented ten terms found in the claims of the patents for construction by the Court. After defendants filed their responsive brief to Rambus's opening claim construction brief, the Court of Appeals for the Federal Circuit handed down an opinion reviewing *ex parte* reexamination of U.S. Patent No. 6,034,918 ("the '918 patent"), also of the Farmwald-Horowitz family, addressing some of the issues disputed here. *See In re Rambus Inc.*, --- F.3d ----, 2012 WL 3329675 (Fed. Cir. 2012). Accordingly, defendants move, unopposed, for leave to file a joint sur-reply addressing that ruling, and Rambus also moves, unopposed to file a response. Those motions are hereby granted, and in consideration of the briefing, the arguments presented at the *Markman* hearing, and for all the reasons set forth below, the disputed terms are construed as follows.

II. BACKGROUND

The Farmwald-Horowitz patents are directed to Synchronous Dynamic Random Access Memory ("SDRAM") chips and related interface and memory control technology. DRAM serves as the primary memory resource for temporary storage and data in use by the Central Processing Unit ("CPU" or "processor"). It is a relatively inexpensive and fast form of temporary memory used in a wide variety of common computer devices. For example, DRAM is used to store display data, and to make information retrieved from the slower hard drive readily accessible to software applications. DRAM cells are composed of one transistor and one capacitor in large, two-dimensional arrays, organized into columns and rows. Each cell stores a bit of data as a small charge, traditionally denoted as "0" for a low-voltage charge, or a "1" for a higher voltage charge. Over time, the capacitors lose their charge, and must be "dynamically" refreshed to preserve the integrity of the stored information. As a consequence of this charge "leaking," DRAM loses information rapidly once the device is turned off, unlike non-volatile memory resources, such as flash memory.

[1] The Farmwald-Horowitz patents all descended from U.S. Patent App. Ser. No. 07/510,898, and share similar written descriptions and diagrams. For simplicity's sake, the Court adopts the parties' convention of referring exclusively to the '916 patent.

Defendants' memory controllers are the accused device in this litigation, and although "controller/controller device" is a disputed claim term, generally speaking, the controller's function is to intermediate between the DRAM assembly and the processor. How precisely it achieves that goes to the heart of the dispute between Rambus and defendants. The memory controller may be integrated into the processor or exist as a separate, standalone chip. In either case, it communicates with the DRAM assembly via a series of traces or wires, commonly referred to as the "memory bus." The bus typically includes a separate "control bus," "address bus," and "data bus." The control bus also specifically includes a "Row Address Strobe" ("RAS") and "Column Address Strobe" ("CAS"), which direct the selection of particular memory cells for "reading" and "writing" operations.

Interposed between the bus and the memory array is a component of the DRAM assembly called the "sense amplifiers." The amplifiers access individual memory cells through "bit line" circuitry to facilitate read/write operations, by amplifying and "loading" the charge information in selected rows of DRAM cells (also called a "page" or "word lines"). To achieve this, the sense amplifiers are "precharged," or primed with an intermediate charge that enables the circuitry to perceive the stored charge (high or low) correctly. Once the row and column are selected, through operation of the control bus, address bus, and sense amplifiers, data is transmitted over the data bus.

Existing "asynchronous" DRAM systems generally perform read operations according to the following chronology: first, the RAS bus transitions from low to high voltage to prompt the sense amplifiers to precharge. It then transitions back to low voltage and holds there, activating and loading a particular row of memory cells into the sense amplifiers. The CAS bus then transitions from high voltage to low, identifying a particular column, which effectively selects a single memory cell. The data stored in that cell is then transmitted over the data bus. Write operations are executed in a similar fashion.

The claims of the Farmwald-Horowitz patents asserted in this litigation are directed to the controller and circuitry that communicates with the DRAM assembly, as well as methods for operating them. Unlike conventional asynchronous systems, the claimed inventions synchronize the

transmission of signals from the controller to the DRAM assembly with a "clock signal" for the purpose of improving the speed and efficiency of operations.

III. LEGAL STANDARD

Claim construction is a question of law to be determined by the Court. *Markman*, 52 F.3d at 979. "Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)). Accordingly, a claim should be construed in a manner that "most naturally aligns with the patent's description of the invention." *Id.*

The first step in claim construction is to look to the language of the claims themselves. "It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). A disputed claim term should be construed in a manner consistent with its "ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1312-13. The ordinary and customary meaning of a claim term may be determined solely by viewing the term within the context of the claim's overall language. *See id.* at 1314 ("[T]he use of a term within the claim provides a firm basis for construing the term."). Additionally, the use of the term in other claims may provide guidance regarding its proper construction. *Id.* ("Other claims of the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment as to the meaning of a claim term.").

A claim should also be construed in a manner that is consistent with the patent's specification. *See Markman*, 52 F.3d at 979 ("Claims must be read in view of the specification, of which they are a part."). Typically the specification is the best guide for construing the claims. *See Phillips*, 415 F.3d at 1315 ("The specification is . . . the primary basis for construing the claims."). *See also Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) ("[T]he

specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term."). In limited circumstances, the specification may be used to narrow the meaning of a claim term that otherwise would appear to be susceptible to a broader reading. *See SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001); *Phillips*, 415 F.3d at 1316. Precedent forbids, however, a construction of claim terms that imposes limitations not found in the claims or supported by an unambiguous restriction in the specification or prosecution history. *Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1347 (Fed. Cir. 1998) ("[A] court may not import limitations from the written description into the claims."); *Comark Commc'ns., Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998) ("[W]hile . . . claims are to be interpreted in light of the specification, it does not follow that limitations from the specification may be read into the claims."); *SRI Int'l v. Matsushita Elec. Corp. of Am.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc) ("It is the *claims* that measure the invention.") (emphasis in original). A final source of intrinsic evidence is the prosecution record and any statements made by the patentee to the United States Patent and Trademark Office (PTO) regarding the scope of the invention. *See Markman*, 52 F.3d at 980.

The court also may consider extrinsic evidence, such as dictionaries or technical treatises, especially if such sources are "helpful in determining 'the true meaning of language used in the patent claims.'" *Phillips*, 415 F.3d at 1318 (quoting *Markman*, 52 F.3d at 980). Ultimately, while extrinsic evidence may aid the claim construction analysis, it cannot be used to contradict the plain and ordinary meaning of a claim term as defined within the intrinsic record. *Phillips*, 415 F.3d at 1322-23. Once the proper meaning of a term used in a claim has been determined, that term must have the same meaning for all claims in which it appears. *Inverness Med. Switzerland GmbH v. Princeton Biomeditech Corp.*, 309 F.3d 1365, 1371 (Fed. Cir. 2002). Several terms disputed in these related actions have already been construed in prior litigation involving other alleged infringers. While the parties agree that those constructions are not binding, and were adopted in consideration of different, allegedly infringing devices, and in some cases without the benefit of the arguments raised here, "uniformity in the treatment of a given patent" is also generally desirable.

Markman, 517 U.S. at 390. Those previous constructions may be viewed as "persuasive and highly relevant." *Verizon Cal. Inc. v. Ronald Katz Tech. Licensing, P.A.*, 326 F. Supp. 2d 1060, 1069 (C.D. Cal. 2003); *Comcast Cable Commc'ns Corp. v. Finisar Corp.*, No. C 06-04206, 2007 WL 1052821 at *2 (N.D. Cal. Apr. 6, 2007) ("Prior constructions may be persuasive, but this Court may reach different conclusions.").

IV. DISCUSSION

No.	Claim term	Rambus's construction	Defendants' construction
1.	controller/controller device	an integrated circuit device that includes circuitry to direct the actions of one or more memory devices	a device that controls one or more devices

The parties debate the appropriate scope of the limitation "controller," or equivalently, "controller device." The dispute focuses on Rambus's suggestions that the claim term refers to (1) "an integrated circuit device," i.e., a single chip device, and (2) that it must control "memory devices," specifically. As defendants note, the term actually only appears in the claims of the '916 patent, not its specification. The specification refers, instead, to "master or bus controller devices, such as CPUs … [which] send[] control signals" and "slave devices, such as DRAM, SRAM or ROM memory devices … [which] respond[] to control signals." The claims, on the other hand, recite a "method of controlling a synchronous memory device by a controller." '916 patent, col. 25:66-67.

Turning to the first point, the parties here have stipulated, consistent with the Federal Circuit's opinion in *Rambus v. Infineon Techs. Ag*, 318 F.3d 1081, 1091 (Fed. Cir. 2003), that "integrated circuit device" means "a circuit constructed on a single monolithic substrate, commonly called a 'chip.'" (*See* Joint Claim Construction and Prehearing Statement (Dkt. No. 95) at 1). Rambus argues that the term "controller" implies that it is an "integrated circuit device" because the specification describes the "Field of the Invention" as follows: "An *integrated circuit* bus interface for computer and video systems is described which allows high speed transfer of blocks of data, particularly to and from memory devices, with reduced power consumption and increased system reliability." '916 patent, col. 1:22-27 (emphasis added). Rambus also points out that the

specification elaborates: "The bus architecture of this invention connects master or bus controller devices, such as CPUs, Direct Memory Access devices (DMAs) or Floating Point Units (FPUs), and slave devices such as DRAM, SRAM or ROM memory devices." *Id.*, col. 6:16-21. Finally, Rambus emphasizes that in the *Hynix* litigation, the parties stipulated that "memory controller" means "[a]n integrated circuit device that includes circuitry to direct the actions of one or more memory devices." (*See* Exh. B to Detre Decl. in Supp. of Opening Br., at 2 (*Hynix I* Joint Claim Construction and Prehearing Statement)). Of course, that is of relatively limited significance.

Defendants in this action argue that nothing in the specification requires the controller, specifically, to be a single chip device. They argue that Rambus could have drafted claims stating that the controller must be formed on a single semiconductor substrate, but did not. Defendants also emphasize that prior art, in the form of U.S. Patent No. 4,315,308 ("the '308 patent" or "the Jackson patent"), discloses a device that controls communications with a memory device, described in the Rambus patents as containing "a single CPU," *see* '916 patent, col. 2:22-31, but actually comprised of "two separate chips." '308 patent, col. 4:22-23, 4:44-47. They therefore argue that the state of the art contradicts Rambus's suggestion that a controller is known within the field as a single chip device. To that point, Rambus replies that the Jackson patent was filed in 1978, and therefore should not be given much weight in assessing the terminology of the art at the time of the invention, many years later. On balance, the controversy over the Jackson prior art is not dispositive.

More instructive is the Federal Circuit's recent opinion in *In re Rambus*, 2012 WL 3329675 at *4, which addresses arguments similar to those advanced here in the course of reviewing on appeal the reexamination of another Farmwald-Horowitz patent (also asserted in this litigation), U.S. Patent No. 6,034,918 ("the '918 patent"). In that matter, the Board of Patent Appeals and Interferences (BPAI), construing "memory device," rejected Rambus's argument that the term necessarily consisted of an integrated circuit device. Upon review the Court agreed, holding that while the claim could be satisfied by a single chip device, it was not so limited: "The specification language Rambus cites shows only that the invention can be carried out with a single chip memory device, it does not require the invention to be so performed. … To the extent Rambus wanted to

limit the memory device to a single chip component, it could have expressly done so. It did not, and this court will not do so here." *Id.*

Recognizing that *In re Rambus* concerned a different claim term, the same logic applies to the debate here over the meaning of "controller." While the '916 patent's specification supports Rambus's view that its claims could be embodied by a single chip device, it does not go so far as to require as much. To hold otherwise would contravene the principle that limitations not found in the claims or supported by an unambiguous restriction in the specification or prosecution history are not to be read into the claims. *Laitram Corp.*, 163 F.3d at 1347. Rambus protests that defendants' alternative suggestion is wholly divorced from the field of the invention, and thus too general. While Rambus is correct that the claims must be construed in light of the specification, and the file history, its suggestion that defendants' proposed construction would potentially cover "the anti-lock brake controller on an automobile, the controller of a back yard irrigation system, and a host of other technologies with no connection whatsoever to the patented inventions at issue here" is greatly overstated. Even with defendants' broader proposed construction of controller, given the context provided by the intrinsic record, a person skilled in the art would plainly understand that the controller is embodied by circuitry, and not some other random form of technology. That understanding may be preserved without importing the further requirement that the controller must be an integrated circuit.

As for the second issue – that is, whether the device directs or controls[2] "memory devices" in particular, as Rambus suggests, or "devices" more generally, as defendants submit – the claims recite a "method of controlling a synchronous memory device by a controller." '916 patent, col. 25:66-67. In fact, all of the asserted claims refer to control of memory devices. Defendants argue the specification teaches that "master or bus controller devices, such as CPUs" are operable with the alleged invention. *Id.*, col. 6:16-17. *See also id.*, col. 6:27-30 ("semiconductor devices, including

[2] Rambus favors the verb "direct" over "control" and argues that the latter, defendants' suggestion, is circular and unhelpful. While "direct" is generally synonymous with "control," because there is no discernible difference, "control" is more faithful to the claims language, and since the word has no demonstrated meaning peculiar to the art, it needs no further construction.

devices, *disk controllers*, or other special purpose devices such as *high speed switches* can be modified for use with the bus of this invention" (emphasis added)). Rambus replies that its proposed construction does not suggest the controller is limited to controlling *only* memory devices, and agrees that a controller may, as the specification suggests, control other devices. If that is so, Rambus cannot credibly object to the inclusion of a reference to control other devices. Accordingly, the first term is construed to mean, "a device that controls one or more memory devices or other devices."

No.	Claim term	Rambus's construction	Defendants' construction
2.	clock signal	a signal that is continuously present and continuously repeats at regular intervals, to provide timing information	a periodic signal that is continuously present and repeats at regular intervals to provide timing information
3.	external clock signal	a signal that is continuously present and continuously repeats at regular intervals, from a source external to the device to provide timing information	a periodic signal that is continuously present and repeats at regular intervals to provide timing information from a source external to the device

The dispute over the second and third terms is relatively limited. The '916 patent describes a two clock system which, together, "provide a synchronized, high speed clock for all the devices on the bus." '916 patent, col. 8:35-36. As their respective constructions suggest, the parties agree that the claimed "clock signal" must be "periodic," "continuously present," "repeat[ed] at regular intervals," and "provide timing information."[3] They further agree that an "external clock signal" is one "from a source external to the device." The parties disagree, however, as to whether a "periodic" signal, by its nature, must be "continuously present" and "continuously repeat[ing] at regular intervals," with Rambus arguing in the affirmative, and defendants countering that a signal

[3] Rambus initially proposed, "a periodic signal, i.e. one that is continuously present and repeats at regular intervals to provide timing information." At the hearing, however, it suggested eliminating the term "periodic" and instead adopting the phrase "that is continuously present and continuously repeats," as the table above reflects. Defendants would not agree to that proposal because it implies that the signal must always be repeating.

may be intermittently periodic, and yet still "continuously present." In other words, the parties agree that, at least during operations, the clock signal must look like this:

Disagreement arises, however, as to whether the signal must always repeat the pattern represented above, as Rambus urges, or may go "flat" at times, as defendants insist.

Neither side relies on the intrinsic record in support of their respective positions.[4] Instead, both look to extrinsic sources of evidence for support. Rambus argues that the lay dictionary definition of "periodic" is "occurring, appearing, or recurring at regular intervals." *Webster's New World Dictionary of American English* 1004 (3d College Ed. 1988). It therefore maintains that a periodic signal is necessarily "repeat[ed] at regular intervals." Rambus also reasons that if the signal is not continuously present, then it cannot possibly repeat at regular intervals, because the pattern would be disrupted by the absence of the signal.

Rambus notes that in another coordinated action in this District, the Court construed "external clock signal" to mean a "periodic signal from a source external to the device to provide timing information" without further glossing the word "periodic."[5] That decision, however, followed a stipulated construction in an earlier *Hynix* case. *Hynix Semiconductor Inc. v. Rambus Inc.* ("*Hynix I*"), No. C 00-20905, 2004 WL 2610012 at *20 (N.D. Cal. Nov. 15, 2004) ("The parties agree that 'external clock signal' should be construed as 'a periodic signal from a source external to the device to provide timing information.'"). In the later, coordinated actions, the Court declined to adopt the alleged infringers' position that the claimed external clock signal must be "continuous." It did so recognizing that "[n]either side has developed this argument to the extent the court feels

[4] Although defendants invoke the '916 patent's specification to provide some general context and suggest that the clock signal must be continuously present, that does not appear to be in dispute.

[5] Those cases are *Rambus Inc. v. Hynix Semiconductor Inc., et al.*, No. C 05-0034 RMW (N.D. Cal.), *Rambus Inc. v. Samsung Electronics Co. Ltd., et al.*, No. C 05-02298 RMW (N.D. Cal.), and *Rambus Inc. v. Micron Technology, Inc., et al.*, No. C 06-00244 RMW (N.D. Cal.).

comfortable determining whether an 'external clock signal' must be continuous." *Rambus Inc v. Hynix Semiconductor Inc.*, 569 F. Supp. 2d 946, 985 (N.D. Cal. 2008). Consequently, that decision is of little assistance.

Defendants here stress that the PTO rejected the position Rambus now urges in its reexamination of the Farmwald-Horowitz patents. *Rambus Inc. v. NVIDIA Corp.*, Appeal No. 2012-000171, BPAI decision on Appeal at 7-8 (June 11, 2012). It held that the claimed clock signal must be continually present "during data inputs to synchronize data transfers," not at all times. *Id.* at 8. Defendants also suggest that Rambus took an inconsistent position before the PTO in reexamination proceedings, stating that the clock signal "is a *continuously present* periodic signal," suggesting that a periodic signal is not, by its very nature, "continuously present." (Exh. D to Cadkin Decl. in Supp. of Defs.' Br. (Reex. App. No. 95/001,169, Decl. of Robert J. Murphy Under 37 C.F.R. § 1.132 at 24 (Sep. 4, 2009))). Rambus responds that defendants have misread the submission to the PTO, and points to other deposition testimony from the same quoted expert suggesting that a periodic signal must be continuous whenever the device is turned on. (*See* Exh. B to Detre Decl. (Dep. of Robert J. Murphy, Apr. 25, 2005) at 127:9-24).

Neither side has identified any persuasive evidence to suggest how a person skilled in the art would understand the term "periodic," or, more generally, "clock signal." In the absence of some greater demonstration by plaintiff, it is not at all self-evident why a periodic signal must, by its nature, be continuously repeating and continuously present. Although Rambus suggests defendants have failed to respond to its argument that a discontinuous signal cannot repeat regularly, that is not entirely accurate. Defendants' position is apparently that of the PTO. They reason a periodic signal may be intermittent, e.g., present during read or write operations, without being always present. Because neither the intrinsic nor extrinsic evidence indicates otherwise, defendants' proposed constructions of "clock signal" and "external clock signal" are hereby adopted.

No.	Claim term	Rambus's construction	Defendants' construction
4.	operation code	one or more bits to specify a type of action	one or more control bits to specify a type of action

The parties largely agree on the appropriate construction of the fourth claim term, as well. Disagreement focuses solely on defendants' inclusion of the phrase "*control* bits" (emphasis added). Rambus maintains "control bits" is not a term of art, and argues the concept of "control" is captured by the phrase, "to specify a type of action." It notes its proposed construction is consistent with that adopted by the Court in the *Hynix I* litigation. *See Hynix I*, 2004 WL 2610012 at *13 ("Therefore, the court finds 'operation code' is properly construed as 'one or more bits to specify a type of action.'"). Defendants respond that the modification of "bits" with "control" was not considered in the earlier case. They maintain there is agreement "operation code" refers to "control information," not "address information" or "data." *See, e.g.,*'916 patent. Col. 4:11-13 (a memory "device[] receive[s] *address* and *control* information over the bus and transmits[s] or receive[s] requested *data* over the same bus" (emphasis added)); U.S. App. No. 09/796,206, Resp. to Office Action at 3 (Nov. 26, 2001) (stating that "operation code" does not include "address information" and refers only to "control information"). At argument, Rambus acknowledged operation code refers to "control information," but nonetheless insists its proposed construction adequately conveys that meaning by stating the bits "specify a type of action." Absent a debate as to whether one skilled in the art would understand "operation code" denotes "control information," then the construction should clearly reflect that, for the benefit of the jury. Because Rambus appears to be correct that "control bits" is not a term of art, the "bits of control information" is a superior formulation. Defendants do not oppose that edit. Accordingly, the term shall be construed to mean "one or more bits of control information to specify a type of action."[6]

No.	Claim term	Rambus's construction	Defendants' construction
5.	precharge information	one or more bits indicating whether the sense amplifiers and/or bit lines (or portion of the sense amplifiers and/or bit lines) should be precharged	ordinary, plain meaning; no construction necessary alternatively, information denoting whether the sense amplifiers and/or bit lines (or

[6] At argument, the Court suggested a clarification that "bits" refers to "bits of information," and the parties did not object. Nonetheless, upon further reflection, it does not appear such elaboration is necessary.

			portion of the sense amplifiers and/or bit lines) should be precharged

The parties' disagreement as to "precharge information" turns, in the first instance, on whether or not the term requires any construction. If Rambus prevails on that preliminary question, the parties agree the function of precharge information is to determine "whether the sense amplifiers and/or bit lines (or a portion of the sense amplifiers and/or bitlines) should be precharged," and disagree whether "information" should be construed to mean "one or more bits indicating…," as Rambus suggests, or "information denoting…," as defendants submit.

On the initial question, defendants argue that because there is basic agreement as to the function of the precharge information, there is no need to construe the term further. They suggest the parties agree precharge information is simply "information" related to the step of "precharging." That argument misses the point: it is not at all self-evident from a lay perspective what the meaning of "precharge information" is, and furthermore, there is some disagreement between the parties as to its precise meaning, as reflected in defendants' position, extensively briefed, that "precharge information" is not limited to "one or more bits" as Rambus insists. Rambus points out, however, "[a] determination that a claim term 'needs no construction' or has the 'plain and ordinary meaning' may be inadequate when a term has more than one 'ordinary' meaning or when reliance on a term's 'ordinary' meaning does not resolve the parties' dispute." *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008). Accordingly, the term cannot simply be left for the jury, as is; it must be construed.

Turning to the parties' proposed constructions, Rambus concedes defendants' proposal is "not necessarily incorrect," but argues that to the extent their construction defines "information" using the word "information," it is circular and unhelpful. (Pl.'s Br. at 15:14-15). Rambus goes on to point out that the specification uniformly refers to the precharge information as consisting of some number of bits. For example the '916 patent specifies that control information is sent to the memory devices in "two 4 bit fields." '916 patent, col. 9:46-47. Rambus notes the parties agree the 4 bit fields of control information include an "AccessType" field that determines the "access mode,"

or in other words, "whether the DRAM should precharge the sense amplifiers or save the contents of the sense amps for a subsequent page access mode." '916 patent, col. 10:47-55. One particular bit of the "AccessType" fields is specified to be the "precharge/save-data switch." *Id.*, col. 11:44.

In response, defendants concede, "certain claims [in the Farmwald-Horowitz family] require 'precharge information' to be represented as 'one or more bits,'" (Defs.' Br. at 13:15-16 (citing U.S. Patent No. 6,564,281 ("the '281 patent"), col. 25:25-27)), but proceed to insist that other claims use the "broader" term "precharge information," which may include "a binary bit." (*Id.* at 13:20-25 (citing U.S. Patent No. 6,751,696 ("the '696 patent"), col. 26:16-24)). The claims defendants rely upon require the precharge information consist of a single bit or "includes a binary bit."[7] '281 patent, col. 25:25-27 ("wherein the precharge information is encoded in the first bit of the operation code"); '696 patent, col. 26:16-24 ("wherein the precharge information includes a binary bit"). It does not follow, as defendants suggest, that the identified claims undermine Rambus's position or somehow imply the claim term must be interpreted more broadly than "one or more bits." As Rambus also points out, the parties similarly agree that precharge information is included in the operation code, which is itself defined as "one or more bits of information," consistent with the Federal Circuit's opinion in *Infineon*. 318 F.3d at 1093 (construing "read" and "write request[s]" as "a series of bits…").

Finally, Rambus emphasizes that the Court in *Hynix I* adopted the construction it urges. While defendants note that, during earlier stages of the *Hynix I* litigation and the later, coordinated actions, Rambus agreed with the Court that precharge information should be construed as "information denoting whether the sense amplifiers and/or bit lines (or a portion of the sense amplifiers and/or bit lines) should be precharged," *see, e.g., Hynix I*, 2004 WL 2610012 at *14-15, the Court in the coordinated actions subsequently revised the construction of "precharge information" to conform exactly to the proposal Rambus advances now. *See* 569 F. Supp. 2d 946 (Appendix A). In view of the foregoing, Rambus has the stronger position on this question:

[7] At the hearing, defendants noted they had identified a single, unasserted claim that did not describe the precharge information in terms of bits. That evidence was not presented in the papers, and is of marginal significance anyway, given that the claim is not at issue.

"precharge information" is construed as "one or more bits indicating whether the sense amplifiers and/or bit lines (or portion of the sense amplifiers and/or bit lines) should be precharged."

No.	Claim term	Rambus's construction	Defendants' construction
6.	register	a storage element or group of storage elements not part of a memory array that can store one or more bits of information	a storage element that can store information

The parties agree that the claim term "register" refers to a "storage element" and the dispute focuses on (1) whether it is separate from the memory array, and (2) whether it stores only bits or, more broadly, information.[8] With respect to the first issue, both parties claim the support of the intrinsic evidence. Rambus primarily objects to defendants' proposal on the grounds that it is so broad as to permit the conflation of the claimed register with the memory array's cells. It notes the title of the '916 patent describes a "[m]emory device having a variable data output length and a programmable register," with the specification further elaborating: "[r]egisters are provided which may store control information, device identification, device-type and other information appropriate for the chip such as the address range for each independent portion of the device." '916 patent, col. 4:23-27. *See also id.* at col. 23:52-54 ("The DRAM memory array is divided into a number of subarrays … Each subarray is divided into arrays [] of memory cells."). If a register were no different than a memory cell in the DRAM array, Rambus reasons, every "memory device" would necessarily entail a multitude of programmable registers. That result is not supported by the specification, which differentiates between the two elements, or by the state of the art. *See, e.g.*, *IEEE Standard Dictionary of Electrical and Electronics Terms* 797 (5th ed. 1993) (defining "memory cell" as "[t]he smallest subdivision of a memory into which a unit of data has been or can be entered….").

[8] Defendants do not address Rambus's inclusion of the phrase "… or group of storage elements…," and therefore may be deemed not to oppose that language. Because Rambus's opening brief adequately supports its contention that the register need not consist of a single storage element, this aspect of its construction may be adopted.

Defendants argue the specification of the '916 patent is silent as to whether the register may be included in the memory array, and emphasize that Figure 15 does not illustrate any registers at all. They note the Farmwald-Horowitz patents claim "a 'memory device' which includes 'an array of memory cells,' as well as separate 'interface circuitry *including* an access-time register…'" (Defs.' Br. at 15:8-10 (citing U.S. Patent No. 5,841,580, col. 25:22-31)), and suggest those two components are "separate and distinct parts of the memory device." (*Id.* at 15:12-13 (citing U.S. App. No. 10/973,268 at Claim 163)). That evidence appears to support Rambus's position that the registry should not be conflated with memory cells. Defendants also point out that a leading technical dictionary defines a "register" as "[a] device capable of retaining information, often that contained in a small subset (for example, one word), of the aggregate information in digital computer," and while there are some similarities between the foregoing definition and the dictionary definition of "memory cell" identified by Rambus, significantly, they are not the same. *See IEEE Dictionary of Electrical and Electronic Terms* 808 (4th ed. 1988). Because neither the intrinsic nor extrinsic evidence support the high level of generality urged by defendants, Rambus' position must prevail.[9]

Turning to the second issue, whether the register should be construed to "store one or more bits of information," or more generally, "store information," Rambus argues the specification supports its position that the information stored in the register may be included in "bytes" (e.g., eight bits) transmitted by the controller to a memory device. '916 patent, col. 10:13-15; *IEEE Dictionary* 118 (1988) (defining "byte" as a "binary string operated on as a unit and usually eight bits long"). Defendants, on the other hand, insist certain claims in the Farmwald-Horowitz require the register to store other types of "information." *See, e.g.*, U.S. Patent No. 5,983,320 ("the '320 patent"), col. 26:15-27; '916 patent, col. 6:34-37 ("device identification (device ID) register [], a device-type descriptor register [] control registers [] and other registers containing other information relevant to that type of device"). While defendants' position is not necessarily incorrect, significantly, they do not suggest such "information" takes the form of something other than bits.

[9] That result comports, again, with the stipulation of the parties in the coordinated *Hynix II* actions.

The weight of the record demonstrates that, in this context, "information" denotes, more specifically, "one or more bits." That appears to be how one skilled in the art would understand references to "information." Accordingly, Rambus's construction of "register" is hereby adopted.

No.	Claim term	Rambus's construction	Defendants' construction
7.	representative of	indicates	ordinary, plain meaning; no construction required

The seventh claim term, "representative of," appears in a variety of contexts. *See, e.g.*, '916 patent, col. 26:3-5 ("…wherein the value is *representative of* a number of cycles of an external clock signal…" (emphasis added)). Rambus favors construing the term as meaning "indicates" because it fears defendants may argue, at a later stage of litigation, that any relationship between two values means one is "representative of" the other, in service of the position that Rambus's patents are anticipated by prior art, an argument asserted in other litigation on the Farmwald-Horowitz patents. It maintains a possible, future dispute over anticipation confirms there is a live disagreement between the parties as to the meaning of "representative of," and again invokes *O2 Micro* to demand a construction of the term. *See* 521 F.3d at 1361.

Of course, potential legal defenses do not have any bearing on the proper construction of the asserted claims, and as defendants rightly point out, Rambus has failed to adduce any evidence to suggest that "representative of" has a peculiar meaning, either within the context of the Farmwald-Horowitz patents or to persons skilled in the art. To the extent the *Hynix I* Court substituted "indicates" for "representative of" in the course of construing various other claim terms, that does not imply, as Rambus suggests, any need to construe the prepositional phrase here.[10] Thus, while there may be a dispute to the extent Rambus requests a specific lay meaning of the term, and defendants insist no specificity is required, there is no cognizable legal basis or compelling evidence in the record to support Rambus's position. Again, a possible anticipation defense in later

[10] Of course, Rambus is free to advance arguments directed to the merits at the appropriate stage of proceedings. It may not, however, rely on language extracted from other cases in support of its proposed construction, without acknowledging the highly context-specific nature of such holdings. *See, e.g., Tehrani v. Hamilton Med., Inc.*, 331 F.3d 1355, 1361 (Fed. Cir. 2003) ("the statement that one item 'represents' another cannot be interpreted so broadly as to include any case in which the two items are related in some way").

proceedings does not mandate a particular construction of a term, absent evidence of what the term ought to mean in light of the claims. Those circumstances distinguish the present case from *O2 Micro*, 521 F.3d at 1361, which concerned a substantive dispute about the meaning of "only if" within the specific context of the claims. Here, no such dispute is apparent, and "representative of" may be equated with the plain, ordinary meaning of the term as it reads in the claims, with no need for further construction.

No.	Claim term	Rambus's construction	Defendants' construction
8.	sample/sampled/ sampling	obtain(s) at one or more discrete points in time/obtained at one or more discrete points in time/obtaining at one or more discrete points in time	capture(s)/captured/capturing

Again, both parties insist their proposed constructions for "sample" and variants thereof find support in the intrinsic record. Rambus maintains its proposed construction is consistent with the specification, the Court's construction in the coordinated *Hynix II* actions, and the ordinary meaning of the term. The specification employs the concept of sampling, often in verb form, to describe, for example, "clocked receivers" that "sample" input signals." '916 patent, cols. 21:61-62, 23:12-14 ("input receivers [] sample the bus clocks just as they transition"), *and* 22:45 (reference to "sample period"). In *Hynix II*, the Court construed "'sample' to mean 'to obtain at a discrete point in time,' 'samples' as 'obtains at discrete points in time,' and 'sampling' as 'obtaining at discrete points in time.'" *Hynix II*, 569 F. Supp. 2d at 988. Rambus offers only a slight variation on that framework, to clarify that sampling may occur at "one or more" times,[11] but not continuously, as it believes defendants' preferred construction implies. The construction adopted in *Hynix II* also derived some support from the *IEEE Dictionary*'s definition of the term "sampling data," that is, "[d]ata in which the information content can be, or is, *ascertained only at discrete intervals of time*." *IEEE Dictionary* 855 (1988) (emphasis added). Defendants argue Rambus's opponents in *Hynix II* failed

[11] Defendants, for their part, do not directly address this addition to the construction adopted in *Hynix II*. Rambus is generally correct, however, that the *Hynix II* Court's construction of the term contemplates – or at least, does not foreclose – sampling at "one or more" points.

to present intrinsic evidence to suggest that the term "sampling" has a meaning distinct from its ordinary and plain sense, and contend they have done so here.

Defendants also make much of the fact that Rambus concedes "'sampling' does involve capturing values of a signal," and, apparently in other proceedings, has interpreted the term "sampling" as referring to "captu[ring] data on the bus." (Defs. Br. at 17:25-27); (Exh. U to Cadkin Decl. at 33). Defendants also note that an Administrative Law Judge of the International Trade Commission (ITC), in the context of construing asserted claims from another group of Rambus patents (the Barth family), characterized "sampling" of data in a write operation as meaning "capture[] data off the data bus." *In the Matter of Certain Semiconductor Chips and Prods. Containing the Same*, Initial Determination on Violation of Section 337, Inv. No. 337-TA-753, at 234 (Mar. 2, 2012) ("the strobe signal 'initiates sampling' of data by the memory device such that the memory device captures valid data received from the memory controller via the data bus"). Such collateral matters, while arguably of some relevance and persuasive weight, are hardly dispositive here. More fundamentally, the difference between "capture" and "obtain" is not so great, and of somewhat marginal significance from Rambus's point of view.

Ultimately, the more significant disagreement between the parties is limited to the frequency and duration of the claimed sampling. On that question, Rambus urges sampling "is well understood in the art to refer to capturing those values only at points in time, rather than, for example, continuously." (Pl.'s Br. at 19:26-28). Unlike *Hynix II*, defendants in this case have identified some intrinsic evidence to suggest the duration and frequency of the sampling procedure may vary, but that is consistent with the ordinary sense of the word, which implies nothing about the required frequency or length of time data must be obtained. Moreover, defendants have not identified any intrinsic evidence to suggest the claimed sampling may occur continuously – a notion that does not comport with the technical or ordinary definition of the word.

Rambus maintains the specification's reference to "sample period" and "sampl[ing] the bus clocks just *as they transition*" (emphasis added), necessarily implies "discrete points of time" rather than continuous "capturing." '916 patent, cols. 22:45, 23:12-14. As noted above, that concept is

also supported by the 1988 *IEEE Dictionary* definition of "sampling data." In reply, defendants insist Rambus's construction is ambiguous. For example, they ask: is a "discrete" point in time instantaneous? Addressing this apparent ambiguity in the record, Rambus answers a "point in time" is basically instantaneous, but insists the patents' references to "sample period[s]" indicate that there is a period of time during which sampling may occur (for example, half of a clock signal), not a duration during which continuous sampling occurs. *See id.*, col. 22:45. Along somewhat similar lines, defendants also correctly note the Farmwald-Horowitz patents describe sampling as occurring at various frequencies. *See, e.g.*, U.S. Patent No. 6,304,937, col. 24:65-67 ("sampling the first portion of data synchronously with respect to a rising edge transition of an external clock signal"). It is not apparent, however, why the term "sample" and variants thereof must necessarily be limited to a particular frequency or duration, as defendants seem to imply. That understanding is not what Rambus urges, and does not appear to be the common understanding of those skilled in the art. As best as can be discerned, defendants so argue merely to cast doubt on the definiteness of Rambus's proposed construction. In any case, the ambiguity identified by defendants may be eliminated by simply replacing "discrete" with "known," which accords the limitation the flexibility it requires. Accordingly, consistent with *Hynix II*, and for all the reasons set forth above, Rambus's proposed construction shall be adopted. "Sample" means "obtain(s) at one or more known points in time."

No.	Claim term	Rambus's construction	Defendants' construction
9.	synchronous dynamic random access memory device	an integrated circuit device in which information can be stored and retrieved electronically, not including a memory controller, that receives an external clock signal which governs the timing of the response to a read request, write request, or operation code and includes one or more arrays of DRAM cells	a memory device in which an external clock signal is used to regulate the timing of device operations

The principal disputes between the parties regarding "synchronous dynamic random access memory device" ("synchronous DRAM device") are: (1) whether a synchronous DRAM device

must be an integrated circuit device, i.e., a single chip device, (2) whether a synchronous DRAM device may include a memory controller, (3) what the requirement a device be "synchronous" entails, and (4) whether it is necessary to specify a synchronous DRAM device includes "one or more arrays of DRAM cells." As an initial matter, it is important to note that synchronous DRAM device does not actually appear in the specification of the asserted patents and only some of the asserted claims.

On the first question, as noted above, and as Rambus's reply brief candidly acknowledges in a footnote, the Federal Circuit's recent reexamination opinion, *In re Rambus*, 2012 WL3329675 at *4-6, squarely rejected Rambus's argument that term "synchronous memory device" is limited by the Farmwald-Horowitz patents, and in particular by the '918 patent, to single chip devices. Nonetheless, Rambus advances virtually the same argument here in connection with the term synchronous DRAM device. As the Court of Appeals explained in *In re Rambus*:

> This court agrees with the Board that the specification does not restrict the invention to single chip memory devices. There are no words of manifest exclusion or clear disavowals of multichip devices—there are only preferred embodiments and goals of the invention that Rambus argues are better met by single chip devices. The specification language Rambus cites shows only that the invention can be carried out with a single chip memory device, it does not require the invention to be so performed.

Id. at *4. Rambus seeks to limit the impact of *In re Rambus* on these actions by emphasizing that the former claim construction opinion pertains to the term "memory device," rather than synchronous DRAM device. While that is true, the Federal Circuit's logic is highly relevant and, ultimately, also applicable here, for the reasons set forth below.

In its opening claim construction brief, Rambus argues – much as it did before the Federal Circuit in *In re Rambus* – that the language and figures in the '916 patent refer to "DRAM chips" and illustrate "DRAM devices" as single chips.[12] *See, e.g.*,'916 patent, col. 3:43-45, *and* Figs. 1, 2,

[12] To the extent Rambus seeks to distinguish *In re Rambus* on the grounds that it construed "memory device" rather than the narrower term, "synchronous DRAM device," the effort fails, given that before the Federal Circuit's order was issued, it took the position *In re Rambus* would "determine whether a memory device, and therefore a synchronous dynamic random access memory device, may or may not include a memory controller, and will be binding here." *See* Pl.'s Br. at 22:18-21. Rambus's simultaneous reliance on intrinsic evidence concerning the term "DRAM device," another partial variant of the term to be construed here, also appears conveniently selective

3, 9, 15. The fact that the Farmwald-Horowitz specifications describe single chip devices as DRAM devices does not, however, compel the converse conclusion that the term "synchronous DRAM device" must be construed as encompassing only single chip devices. Without "manifest exclusion or clear disavowals," such a limitation may not be imported from the specification into the claims. *In re Rambus*, 2012 WL3329675 at *4. While Rambus seeks to characterize the BPAI's decision below in *In re Rambus* as helpful, that opinion is of very limited assistance to it. *See* BPAI Decision on Appeal, Appeal 2010-011178, at 29 ("As the Examiner further noted, Appellant directed at least one claim more narrowly to a 'memory (DRAM) device in claim 3 of U.S. 5,841,715, thereby implying a memory device is broader than a chip.").

Notably, the Federal Circuit's opinion in *In re Rambus* comports with the District Court's holding in *Hynix II*. In *Hynix I*, construing the term "synchronous memory device," the District Court accepted the parties' stipulated construction of "memory device" as "an integrated circuit device in which information can be stored and retrieved electronically," and focused instead on the disputed meaning of the modifier "synchronous." 2004 WL 2610012 at *6-8. In *Hynix II*, the Court had occasion to revisit the meaning of "memory device" to resolve "whether a 'memory device' incorporates the definition of an "integrated circuit device," and with it, the single chip limitation from *Infineon.*" Like the Federal Circuit in *In re Rambus*, the District Court ultimately concluded: "[b]ecause the specification does not clearly limit the scope of the invention to a single chip, the court declines to read the phrase 'memory device' so narrowly. … A 'memory device' is 'a device in which information can be stored and retrieved electronically.' It need not be on a single chip." 569 F. Supp. 2d at 973. Rambus seeks to limit all these unfavorable rulings as construing different claim terms, *but see supra* note 12, and instead emphasizes the passing observation of the District Court in *Hynix II*, that claims directed to "a method of operation of a synchronous dynamic random access memory device" apparently reflect "limits on the scope of 'memory device' … demonstrating that Rambus knew how to limit its claims to a single chip when it wished to do so." *Id.* at 974. That passage is of limited import: "synchronous DRAM device" was not construed in

and fundamentally inconsistent with its position that "synchronous DRAM device" must be understood entirely distinctly.

Hynix II, and other than the quoted passage, the opinion does not explain how the foregoing conclusion was drawn.

Defendants on the other hand, stress Rambus has taken supposedly inconsistent positions in the course of litigating its many cases, variously construing "synchronous DRAM device" as "a synchronous semiconductor device which includes one or more arrays of DRAM cells," or "a dynamic random access memory device that receives an external clock signal which governs the timing of a response to the transaction request." (Defs.' Br. at 20 n.16). Defendants also advance an argument they raised in connection with the term "controller/controller device," above: that is, had Rambus acted as its own lexicographer to limit expressly the claim term "synchronous DRAM device" to one which is "formed on a single semiconductor substrate" or consists of an "integrated circuit device," its proposed construction might be supportable. It has not done so, of course. *See also In re Rambus*, 2012 WL 3329675 at *5 ("memory devices 'formed on a single semiconductor substrate' are properly limited to single chip devices").

Ultimately, then, on this first question, defendants must prevail. The intrinsic record does not support limitation of "synchronous DRAM device" to an integrated circuit device. First, the claims do not suggest any such thing. As the Federal Circuit and *Hynix II* observed, Rambus certainly knew how to claim a single-chip device and did not employ language in drafting its claims indicating such intention. Second, the specification does not contain a clear disavowal of multi-chip devices sufficient to support such a narrowing of Rambus's claims. *See In re Rambus*, 2012 WL3329675 at *4 ("There are no words of manifest exclusion or clear disavowals of multichip devices—there are only preferred embodiments and goals of the invention that Rambus argues are better met by single chip devices."). Consistent with the logic employed by other Courts, here, Rambus's suggestion that "synchronous DRAM device" must be "an integrated circuit device" must be rejected.

The next point of disagreement concerns whether or not a synchronous DRAM device may include a memory controller. *In re Rambus* sheds some light on that question, as well, if only, again, indirectly. Before the BPAI and the Federal Circuit, Rambus categorically argued the term

"memory device cannot include a memory controller," *id.* at *7, a position both the agency and the Court rejected:

> Rambus's construction broadly excluding any memory controller that provides more functionality than simple control logic fails. … In fact, the claims [of the '918 patent] expressly calls for the memory device to provide the control functionality of receiving block size requests and outputting specific amounts of data. Nothing in the claim prevents the memory device from consisting of a storage chip and a device that facilitates the receiving and outputting from that storage chip.

Id. The Court then went on to hold that a "memory device," as the term is used in the Farmwald-Horowitz patents, "may have a controller that, at least, provides the logic necessary to receive and output specific data, but does not perform the control function of a CPU or bus controller." *Id.*

Rambus's opening claim construction brief conceded the Federal Circuit's opinion would control this issue. (*See* Pl.'s Br. at 22:18-21). In light of the result reached by the Court of Appeals, Rambus now insists CPUs and bus controllers may not be included in a synchronous DRAM device. Defendants also rely on *In re Rambus*, but contend a "memory controller" indeed "provides the logic necessary to receive and output specific data," and therefore may be included in the synchronous DRAM device. Consistent with both parties' views, the term may be construed in accordance with the Federal Circuit's opinion to specify a "synchronous DRAM device" "may have a controller that provides the logic necessary to receive and output specific data, but does not perform the control function of a CPU or bus controller."

Turning to the third point of contention, the parties agree a synchronous DRAM device must use an external clock for timing purposes, but disagree as to how that component of the device should be described. Rambus proposes "device … that receives an external clock signal which governs the timing of the response to a read request, write request, or operation code," whereas defendants submit, more simply, "device in which an external clock signal is used to regulate the timing of device operations." Rambus attacks defendants' suggestion as vague as to whether, for example, all operations are regulated by the clock, or if not, which ones. Rambus rightly points out defendants' construction leaves it unclear how the device uses the clock signal to regulate the timing of operations if it is not "received." Finally, Rambus also claims the support of the *Hynix I* claim

construction, which construed "synchronous memory device" as "a memory device that receives an external clock signal which governs the timing of the response to a transaction request." 2004 WL 2610012 at *6-8. In its proposed construction, Rambus has substituted "a read request, write request, or operation code" in place of "transaction request," because the latter term is not included in any of the asserted claims in this case.

Defendants respond that a construction requiring the synchronous DRAM device to *receive* a clock signal will render some claim language superfluous. *See, e.g.*, U.S. Patent No. 6,324,120, col. 26:30-34 (claiming a "method of operation of a synchronous dynamic random access memory device[,] … the memory device comprising: clock circuitry to receive an external clock signal"), *and* '696 patent, col. 24:58-61 (reciting a "synchronous memory device … [which] comprises: clock circuitry to receive an external clock signal"). There does not appear to be much dispute, then, as a substantive matter, that the claims invoke reception of the clock signal. The transitional phrase "comprising," however, suggests the synchronous DRAM device includes "circuitry to receive an external clock signal," precisely as Rambus suggests.[13] Although defendants also insist Rambus has, in other proceedings, generally supported their suggestion the clock signal is used to regulate the timing of device operations, that advocacy, is not strictly inconsistent with the position it urges here.

Finally, defendants argue Rambus's construction of a synchronous DRAM device as "includ[ing] one or more arrays of DRAM cells" is redundant and unhelpful, given that there is no disagreement a synchronous DRAM device is a variant of a DRAM device and must include one or more DRAM memory arrays. Rambus does not directly dispute that fair point. Accordingly, the term "synchronous DRAM device" is construed as "a memory device in which information can be stored and retrieved electronically, and which uses an external clock signal to regulate the timing of device operations. It may have a controller that provides the logic necessary to receive and output specific data, but does not perform the control function of a CPU or bus controller."

[13] As Rambus also points out, the "clock circuitry" limitation is an antecedent to other claims, and therefore actually not redundant.

No.	Claim term	Rambus's construction	Defendants' construction
10.	synchronously with respect to	having a known timing relationship with respect to	operating in step (or in phase) with respect to

The parties' disagreement as to the appropriate construction of the final term is limited to the meaning of "synchronously," with Rambus insisting it means "having a known timing relationship…," and defendants submitting, alternatively, "operating in step (or in phase)…." As an initial matter, the parties debate the implications of defendants' proposed construction. Rambus maintains the phrase "or in phase" suggests the timing of operations must be in phase with the clock, as "in phase" is offered as synonymous with "in step." Defendants responded that is not so, given the conjunction "or," and at the hearing, offered to eliminate the parentheses in their proposed construction to memorialize such understanding. In any case, the larger question is whether or not such a specific construction of the root "synchronous" is appropriate, given Rambus's much more general construction, "having a known timing relationship…."

The parties dispute the significance of the intrinsic record. Rambus argues Figure 13 of the '916 patent makes clear the delay line output signals designated 107 and 108, which are "synchronized with the two bus clocks," are not "in phase" with them, but are instead "phase-shifted" so that the outputs are timed to correspond to the rising and falling edges of the second bus clock. '916 patent, col. 23:14-22. Defendants reply Rambus has misrepresented the function of the output signals, because Figure 13 represents the timing diagram for "how the internal device clock is generated from two bus clock signals using a set of adjustable delay lines." '916 patent, col. 5:19-21. Defendants insist it is the internal device clock which must ultimately be synchronized with the bus clocks to facilitate read and write operations. *Id.*, col. 23:13-24. While that may be the broader point of the alleged invention, the term "synchronized" is used in both contexts, in broader fashion, and in contravention of defendants' understanding of the term.

Defendants also maintain the file history supports their view of the term. Specifically, they argue Rambus responded to the PTO's rejection of claims that required "providing a first portion of the first amount of data to the memory device synchronously with respect to a first transition of an external clock signal," by arguing the claimed operation was "synchronous," in the sense that data

was provided "synchronously with respect to falling edges of the true and complement internal device clocks…." U.S. App. Ser. No. 09/510,213, Response to Office Action at 3 (Aug. 31, 2000). Defendants insist this reflects an understanding of "synchronously" as something more than "a known timing relationship," but rather something closer to "in step." Defendants' position is unpersuasive. Rambus's argument to the PTO does not circumscribe the meaning of "synchronize;" it merely limits the timing relationship with respect to that particular limitation.

Ultimately, it is clear the term is used to describe a variety of timing relationships in the Farmwald-Horowitz patents. It would therefore be inappropriate to limit the term as defendants suggest, without unambiguous support from the specification. Both parties invoke various definitions found in technical dictionaries, but those do not suggest persons skilled in the art have a consistent understanding of the term distinct from the plain and ordinary meaning. *See, e.g., IEEE Dictionary* 978 (1988) (defining "synchronization" as requiring "fixed phase relationship"); *Illustrated Dictionary of Electronics* 537 (4th ed. 1998) (defining "synchronous" as "condition of operating in step (phase) with some reference"). Nonetheless, given the parties' apparent disagreement as to the meaning of the term, some construction is required. *O2 Micro*, 521 F.3d at 1361.

While the parties raise additional arguments, they shed no further light on the issue.[14] Accordingly, Rambus's construction shall be adopted: "synchronously with respect to" means "having a known timing relationship with respect to."

V. CONCLUSION

The disputed claim terms of the patents-in-suit are hereby construed as set forth above. Where the order has identified terms that may require further construction, such matters shall be

[14] Yet another quarrel arises as to whether defendants' construction permits any margin of error, with Rambus arguing that it does not, contrary to the reasonable expectations of one skilled in the art, and defendants insisting that their construction simply minimizes the imprecision or "skew," consistent with the specification. '916 patent, cols. 19:4-9, 23:37-39. There being no real and discernible disagreement on this point, it need not be resolved.

presented, if it becomes necessary, in the context of any dispositive motions or at the time of formulating jury instructions.

IT IS SO ORDERED.

Dated: 9/26/12

RICHARD SEEBORG
UNITED STATES DISTRICT JUDGE